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Custom Back-Side Illuminated Frame Transfer Charge Coupled Device (CCD): Chip Design and Electro-Optical Characterization

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Abstract

This study provides a comprehensive overview of the chip design and electro-optical characterization of a Charge Coupled Device (CCD). While CCD technology is well-established, there are limited research articles that offer holistic perspective of CCD chip development, covering aspects ranging from device architecture and chip layout design to characterization and optimization of electro-optical parameters. In this study, we present CCD chip design and characterization of a custom 1200×256 pixels, frame transfer, Back Side Illuminated (BSI) device. The photosensitive pixels in this device have two phase architecture with 32 µm×32 µm pixel size and shielded anti-blooming to prevent charge spill-over after saturation. The device architecture and design optimization at block level as well as full chip level are presented to achieve the targeted device performance. Furthermore, device electro-optical performance evaluation, characterization and optimization of Chip-On-Board (COB) packaged detector is also presented in this study. While the COB level evaluation of detector performance parameters aligns closely with the designed values, problem was encountered concerning the lower Full Well Capacity (FWC). A unique method was used to investigate the FWC limiting section utilizing signal charge binning. The substrate bounce is identified as a root cause for lower FWC and by clock level optimization, targeted FWC is achieved.

Keywords: CCD, BSI, charge binning, FWC, substrate bounce, chip design, characterization

INTRODUCTION

Charge Coupled Device (CCD) and CMOS Image Sensor (CIS) are silicon based image sensor technologies for Visible and Near Infra-Red (400 to 1000 nm) wavelengths of electromagnetic radiation. Though CIS is mostly used in commercial market, CCDs are extensively used by scientific community for space based remote sensing and astronomical observation [1, 2]. The reduction in instrument size, weight, and power that naturally comes with CIS, compared to CCD solutions, can be substantial. However, the cost and schedule currently needed to develop a new large area CIS is prohibitive to many cost/schedule constrained missions. The CCD sensors still prevalent in niche set of space missions where high quantum efficiency, high frame rate, high full well [2], high Modulation Transfer Function (MTF), high fill factor, High Dynamic Range [3], and low noise is required [4]. Despite the significant advancements made in CCD technology since its initial demonstration at Bell Laboratories, there are scarcity of publications that comprehensively delve into the details of CCD design, characterization, and optimization. The fundamental structure of a Front

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Side Illumination (FSI) and Back Side Illumination (BSI) CCD is shown in Figure 1. In FSI device, the bulk silicon substrate is either p-type or n-type having thickness of 600–700 µm. The various fabrication processes for device take place within a shallow depth of 10–20 µm at upper surface, called photosensitive region or epitaxial layer [5]. This is where photo-electron generated by incident photons are collected and transported. On the upper surface of epitaxial layer, the thin isolating oxide (sometimes supplemented with a thin nitride layer) layer is created, which serves as gate dielectric. The polysilicon gate electrodes are deposited on top of gate dielectrics.

The dielectric layers and metal tracks are deposited on top of polysilicon electrodes to make low resistive connection between gate electrodes and die pads. The BSI devices are fabricated post processing of a FSI device. To fabricate BSI device, a mechanical support wafer (bottom of BSI CCD structure) is attached after FSI fabrication and bulk substrate is removed by chemical/mechanical polishing [6]. In BSI device, the absorption of shorter wavelength by polysilicon electrodes is eliminated as photons incident through back side and are directly absorbed by photosensitive region hence have better Quantum Efficiency (QE) compared to FSI devices at shorter wavelengths [7].

The CCD detector discussed in this study is developed for space based hyperspectral imaging in visible and near infra-red wavelengths (400 to 1000 nm). The desired detector format is 1200 pixels in spatial direction by 256 pixels in spectral direction with pixel size of 32 µm×32 µm. The requirements for quantum efficiency are ≥30% at 400 nm and ≥20% at 1000 nm along with ≥30% at intermediate wavelengths. The pixel Full Well Capacity (FWC) of ≥1 Me^- is required to meet the Signal to Noise Ratio (SNR) requirement of >700.

The target specification for smear during image to storage region fast transfer is <1% with frame time of 36 ms. To achieve the QE requirement at shorter wavelengths, a full depleted BSI CCD process is selected. On the other hand, to achieve the desired quantum efficiency at longer wavelengths, a thick epitaxial layer (50 µm) has been selected in order to absorb the longer wavelength photons.

Additionally, an anti-etalon grooving technique is implemented on the front surface of the device [8]. This approach helps in reducing reflection losses and ensuring the desired quantum efficiency at higher wavelengths.

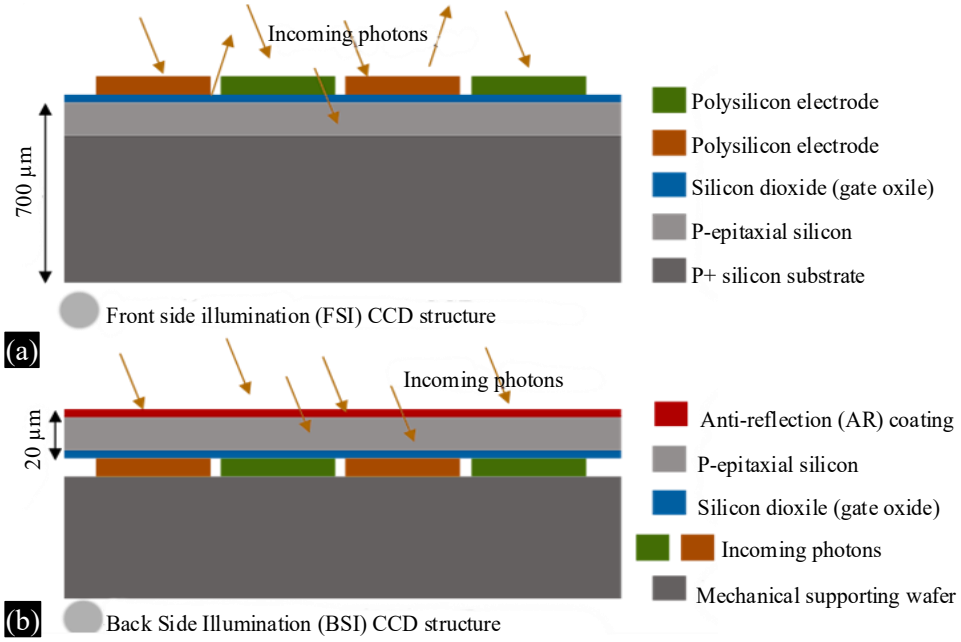

Figure 1. Typical layer structure for (a) FSI CCD detector; (b) BSI CCD detector.

CHIP DESIGN OF CCD IMAGE SENSOR

CCD Chip Architecture

Figure 2 shows the CCD device architecture. The device is designed according to 4-poly-2-metal CCD process flow. The inception of detector design involves meticulous selection of the fabrication process and device architecture to achieve the targeted detector electro-optical performance. The CCD chip design requires optimization and trade-offs of various design parameters to meet system performance while taking care of electrical, optical and thermal attributes at the same time accounting for semi-conductor device physics. The fast transfer of signal charge from image to storage region at 1.4 kHz is required to meet smear requirement of <1% with Full Well Capacity (FWC) of more than 1 Me^{-}. The polysilicon has nearly three order higher resistivity than that of metal tracks, which lead to higher RC delay in clock signals. The fast transfer requires metal strapping to polysilicon electrode to reduce the resistance so that clock fidelity is maintained at high frequency. The design rule for metal layer in foundry process imposes a constraint of two-phase image pixel architecture, on the other hand, higher FWC requires multiphase pixel architecture to secure a larger effective charge storage area [9]. To meet fast transfer requirements, the device architecture is modified so that imaging area is partitioned into two equal upper and lower sections which effectively halves the fast transfer rate. In addition, the two phase image pixel architecture has been designed to allow metal strapping to polysilicon electrodes as per design rule which further improved the clock fidelity for fast transfer. On the other hand, to cater to FWC requirements, we have designed two phase pixel structure with wider storage electrode than barrier electrode as shown in Figure 3 along with thin dielectric and high voltage process [10, 9]. Moreover, the image pixel design incorporates shielded anti-blooming which has superior signal collection and storage capacity compared to gated anti-blooming configuration. Similarly, various possibilities of image pixel design, Horizontal Shift Register (HSR) and bus design, number of output ports are explored in device block level architecture to meet the detector performance requirements.

There are 256 rows and 1200 column of image pixels to cater spectral range and spatial swath requirements respectively. The charges generated in upper 128 image rows are transferred to upper storage region while charges generated in lower 128 image rows are transferred to lower storage region. There are 10 isolation rows between the image and storage sections to reduce light leakage to storage region. On each side of device, there are 16 isolation columns.

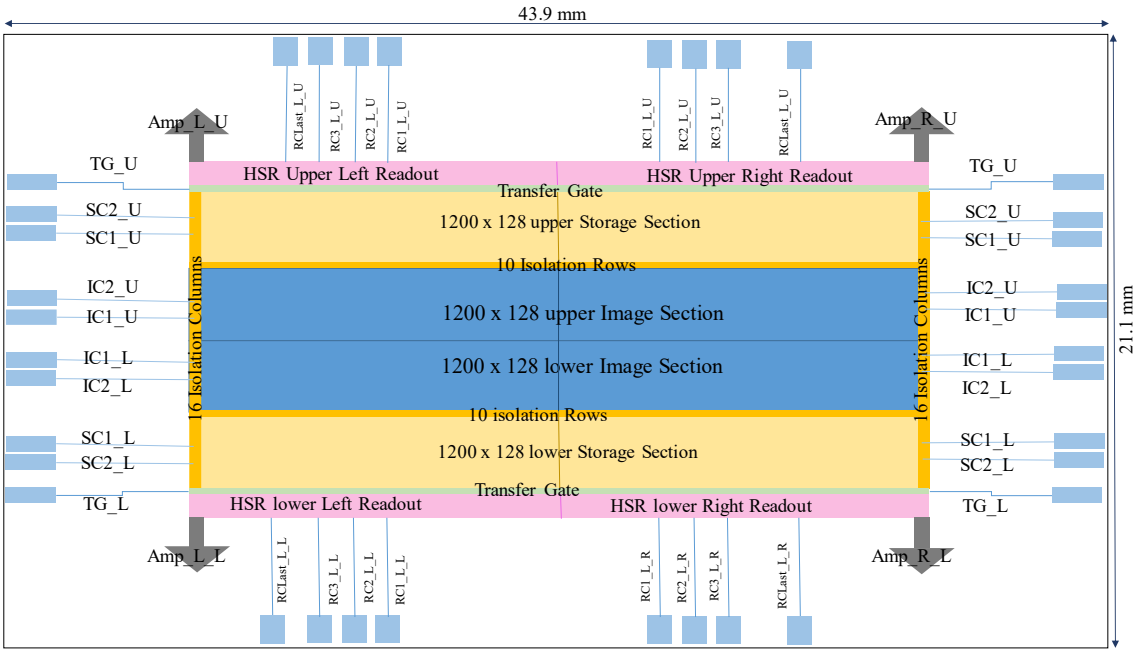

Figure 2. CCD device architecture.

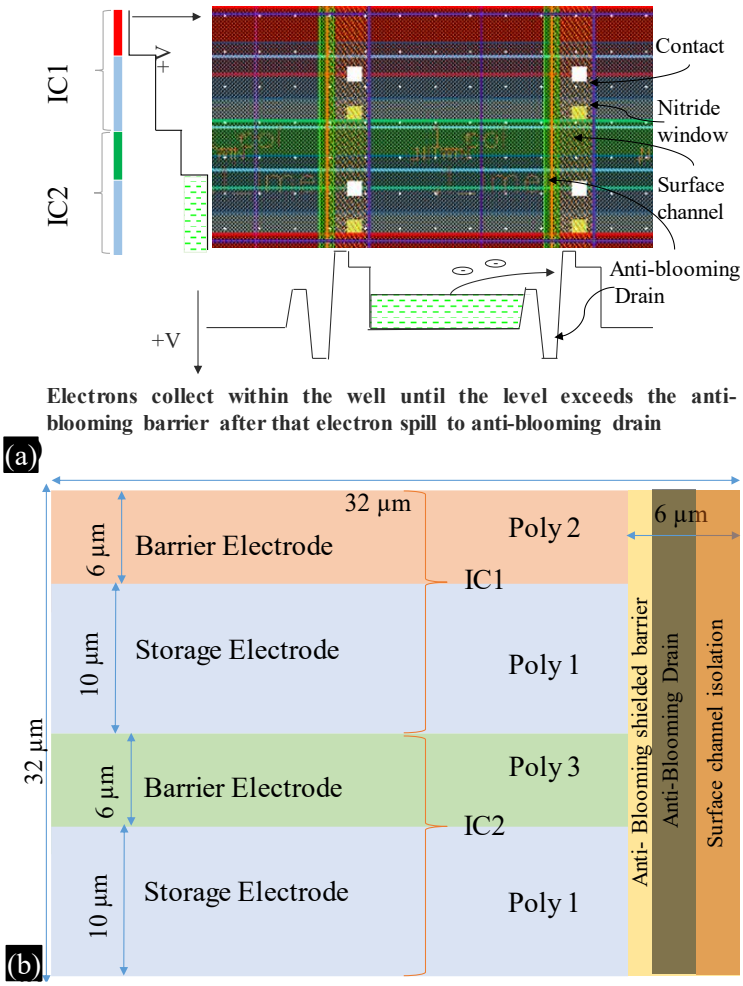

Figure 3. Image Pixel Layout and Potential Diagram under different structure.

The charges stored in both the upper and lower storage region are transferred to the respective Horizontal Shift Registers (HSR) via Transfer Gates (TG). Each HSR is divided into left and right shift registers. Finally, the signal from shift registers are serially transferred towards output section.

Imaging and Storage Pixels Design

The imaging pixel has size of 32 µm×32 µm with lateral shielded anti-blooming. The column isolation between adjacent pixels is 6 µm as depicted in Figure 3. Each phase has channel length (along the charge transfer direction) of 16 µm and width 32 µm, constructed from two poly electrodes. In this two-phase architecture, Poly1 acts as storage electrode while either poly2 or poly3 serves as the barrier electrodes within each phase, as shown in potential diagram of Figure 3(a). While signal integration, the phase 2 is ON and phase 1 is in OFF state. Each pixel has anti-blooming structure, which drain out excess charges over FWC of pixel. The anti-blooming drain is shielded by p-type barrier (Figure 3) to eliminate direct draining of signal electrons, this type of anti-blooming architecture is called shielded anti-blooming. The shielded anti-blooming is also less susceptible to ionizing radiation compared to gated anti-blooming [11, 12]. As the substrate is removed for BSI CCD, at long wavelengths (>850 nm) the absorption length of light in the silicon becomes longer than the CCD thickness. Optical interference then occurs between the light reflected from the front and back surfaces of the CCD. This give rise to 'ripples' in the spectral response of the CCD when measured with narrow band illumination.

This effect is minimized in part by the use of an antireflection coating on the back surface giving low reflectivity at long wavelengths and further reduced by the anti-etalon grooving of front surface of CCD

as reported in the article by Hu *et al.* [8]. The process is based on changing the thickness of the silicon in one half of each pixel so that it is ¼ wavelength thinner than the other half at the wavelength for which the fringing is most critical. The spectral response ripples for one half of the pixel are then in antiphase with those of the other half and cancel, significantly reducing the magnitude of the ripples. The image and storage pixels also has aperture in nitride layer (nitride window) which will be useful in passivation of silicon dangling bonds when annealed with hydrogen gas at elevated temperature.

The vertical potential diagram and the potential along the storage phase in the horizontal directions is shown in Figure 3(a). As signal electrons accumulate up to barrier of anti-blooming, any excess charge beyond this threshold is drained into the anti-blooming drain. The anti-blooming drain from each column needs to be connected to a metal bus which will further connect to a pad. Due to split image section architecture and metal strapping to poly gates, the anti-blooming drain metal bus connection posed a challenge in design. The Design Rule Check (DRC) for metal is 8 µm width and 8 µm spacing. So, if anti-blooming drain metal bus connection is done in image area, the image phase needs to be elongated to incorporate one extra metal track, and pixel buried channel needs to be narrowed to accommodate anti-blooming drain contact on column isolation. This would lead to change in pixel area and responsivity of that particular image row. To circumvent this, the anti-blooming drain metal bus is designed at first storage row adjacent to transfer gate as shown in Figure 4. The ABD contact is placed on column isolation of phase1 (Storage Clock1). As substrate from a back illuminated CCD is removed, the ground connection (substrate) has to be dependent on high resistivity epitaxial layer. To provide low resistance path signals, each columns has P+ substrate connection below transfer gate as shown in Figure 4.

The CCD performance is susceptible to various space radiations and high energy particles. It is reported that if dual gate dielectric (oxide + nitride) is used, the flat band voltage shift due to radiation and high energy particle can be reduced significantly [13]. In this specific device, the approach of dual gate dielectric has been adopted. The implementation of implanted shielded anti-blooming structure in this device has minimal effects of radiation. The storage pixels share a similar structural design, albeit with the distinction of being shielded by a shield metal. Unlike the image pixels, anti-etalon grooving is not implemented in the storage pixels.

The image and storage clock resistance and capacitance was extracted from layout using foundry's extraction software. The image clock has resistance of 20 Ω and capacitance of 8.4 nF with respect to substrate and 2.4 nF interphase capacitance.

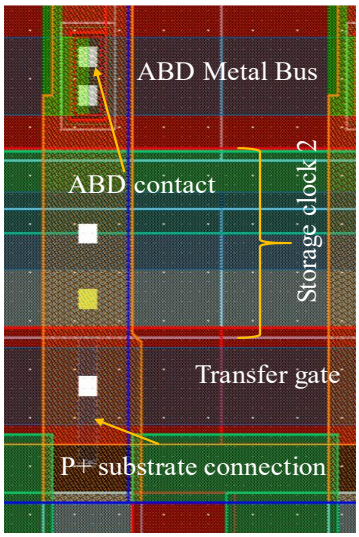

Figure 4. Anti-Blooming Drain (ABD) bus connection in storage region.

The equivalent lump model for image clock propagation is modelled and Figure 5 shows the image clock waveforms at input of device pad (green color) and middle of the device (red color). The image clock has time period of 1.58 µs so that smear in fast transfer is less than 1%. The waveform shows that clock signal has adequate settled duration and voltage swing at 1.58 µs image clock period.

Horizontal Shift Register (HSR) Design

The signal electron from storage region are transferred to Horizontal Shift Register (HSR) through transfer gate. The HSR pixel has three phase architecture as depicted in Figure 6. During charge transfer from storage region to HSR, both phase 1 and phase 2 are ON to collect the signal while phase 3 is OFF to provide isolation between HSR pixels.

Subsequently, the signal charge is serially transferred to output node. Each HSR pixel has 1.5 times FWC than that of image and storage pixel. There are 1232 HSR elements at upper and lower side of the device. Out of these, 616 HSR pixels are readout from the left and additional 616 pixels from the right.

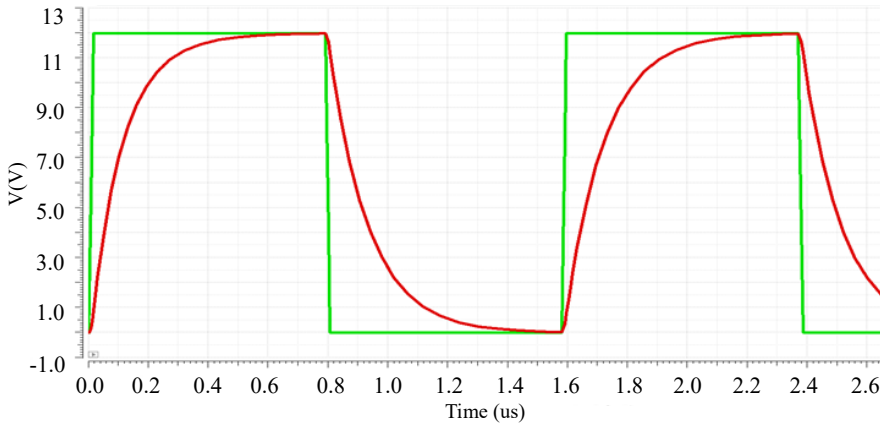

Figure 5. Image clock waveforms, the green color waveform is clock input at pad and red color waveform is image clock at middle of the device length. The horizontal axis represents time in microseconds and vertical axis shows clock voltage.

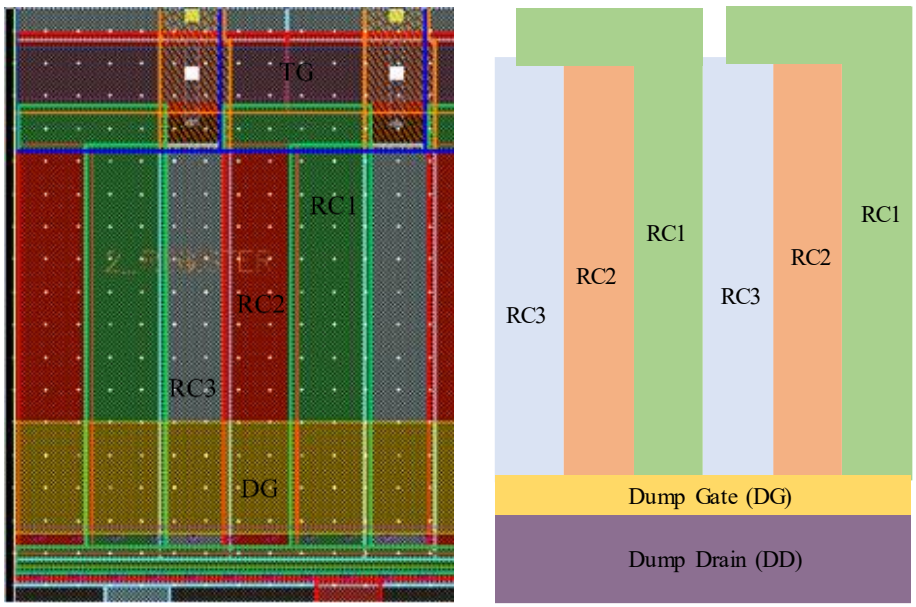

Figure 6. Horizontal Shift Register (HSR) and Transfer Gate (TG) layout. RC1, RC2 and RC3 represents phase 1, phase 2 and phase 3 of three phase architecture.

There is dump gate and dump drain designed beside the HSR to dump the signal charges, if readout is not required. The last HSR electrode is routed to separate pad to reduce signal RC delay which allows proper settle duration of video waveform for efficient charge transfer.

Output Section and Peripheral Circuit Design

The output section comprises the Floating Diffusion (FD), reset transistor, and source follower amplifier while the peripheral circuits consists of guard-ring, substrate ring, routing and bond pads placements. Each set of HSR terminates to an output section as shown in Figure (a).

There are a total of 16 pre-scan HSR pixels. The last few elements of the HSR are tapered to reduce the register width, enabling signal flow to a low capacitance charge detection node. The charge signal from HSR is transferred to highly sensitive capacitor called floating diffusion through output gate. Output gate is maintained at fixed low potential to allow potential gradient.

The output amplifier is Teledyne-e2v proprietary two-stage AC-coupled buried channel amplifier [1]. The second stage requires an external resistive load. The layout of output section is shown in Figure (b).

The CCD active region is surrounded by N+ guard-ring to prevent spurious charge to mix-up with the signal charge of CCD active region. The device has inner p+ substrate ring and outer p+ seal ring, connected to substrate potential. The p+ rings provide low resistive substrate reference potential for electric signals. Each clock is connected to separate bond pad through metal tracks. The clock signal pads are equipped with ESD protection diode. The designed device dimension is 43.704 mm in spatial direction and 21.1445 mm in spectral direction. The device size is larger than the available single reticle size at foundry, so the full device is fabricated by stitching three sub-fields while lithography. The GDS file of designed CCD layout was sent to foundry for wafer fabrication.

ELECTRO-OPTICAL CHARACTERIZATION AND OPTIMIZATION

The detector die from fabricated wafers are proto packaged in the form of Chip-On-Board (COB) for EO characterization. The image of a Back Side Illuminated COB devices is shown in Figure 8. The dark blue region in center of detector is imaging photosensitive region where shield metal has not been deposited. The outer region of die features bond pads that are connected via wire bonds to corresponding pads on COB PCB.

The Figure 9 shows the detailed clock signal timing diagrams and inter-clock relations. The frame time to integrate charge and readout is 36 ms. The pixel readout rate (amplifier rate) is 2.5 MHz. As shown in timing diagram, frame sync OFF duration (35.5 ms) defines the integration time; in this duration, IC1 is OFF and IC2 is ON, hence signal charges collect under IC2 electrodes. After integration, signal charges are transferred to storage region rapidly (referred as fast transfer). After fast transfer, the image section is ready for signal integration for next frame, while readout of signal from storage region occurs at slow rate. One-line time is 260 µs, out of which 10 µs is used for signal transfer from storage to HSR and 250 µs is used for reading 625 pixels. The transfer gate ON duration is 2 µs during storage to HSR signal transfer. The HSR clock period has clock period of 400 ns (2.5 MHz) during sequential line readout. Out of total 625 pixels per line, 16 pixels isolation pixels and 9 extra pixels' readout is used for HCTI calculation. The drive electronic cards to provide electrical stimuli (clocks and biases) and perform detector data acquisition are custom developed. The electro-optical test bench and drive electronic boards are shown in Figure 9. The bias board generates required regulated voltages for detector biases and clocks' high level. The DUT board hosts clock wave-shaping circuits, detector and FPGA responsible for generating clock signal required for detector operation [14]. The acquisition board performs sampling of output signal and converts analog signal into a digital one. The functionalities of these drive electronic boards are thoroughly validated with regards to clocks and bias parameters and their variability.

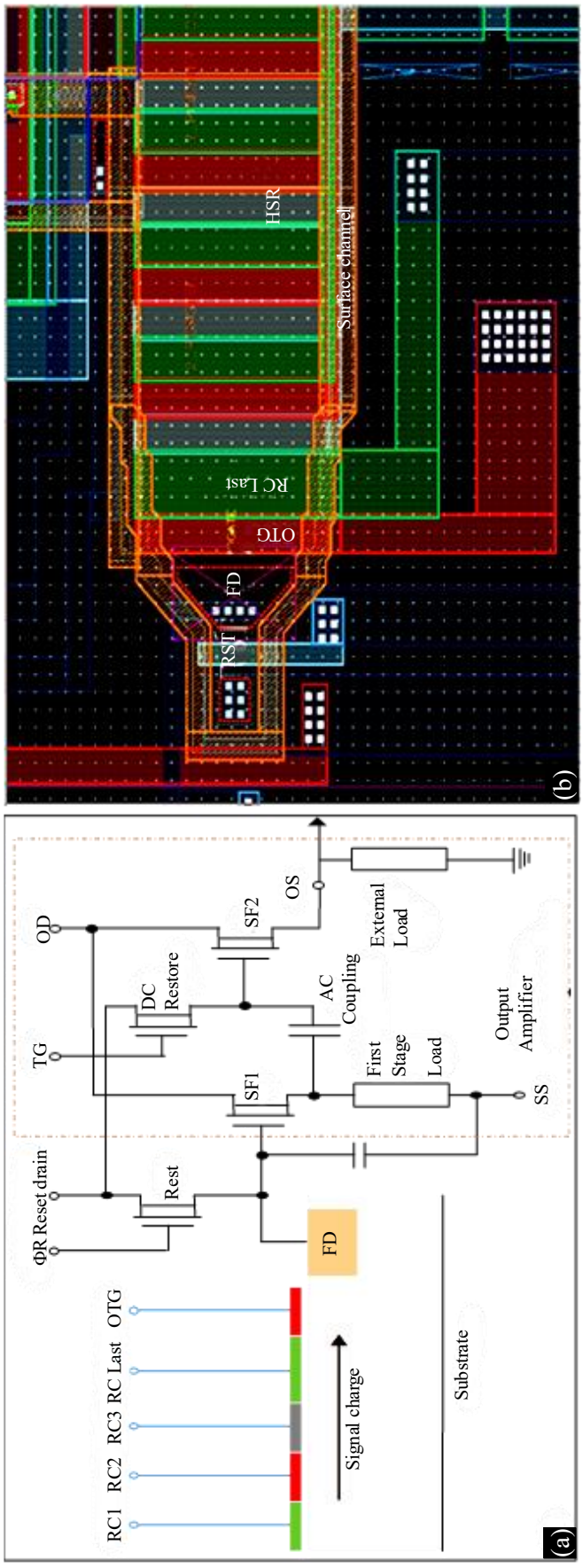

Figure 7. (a) Schematic of Output Section, (b) Output Section layout consisting last register clock (RCLast), Output Transfer Gate (OTG), Floating Diffusion (FD) and Reset Transistor (RST).

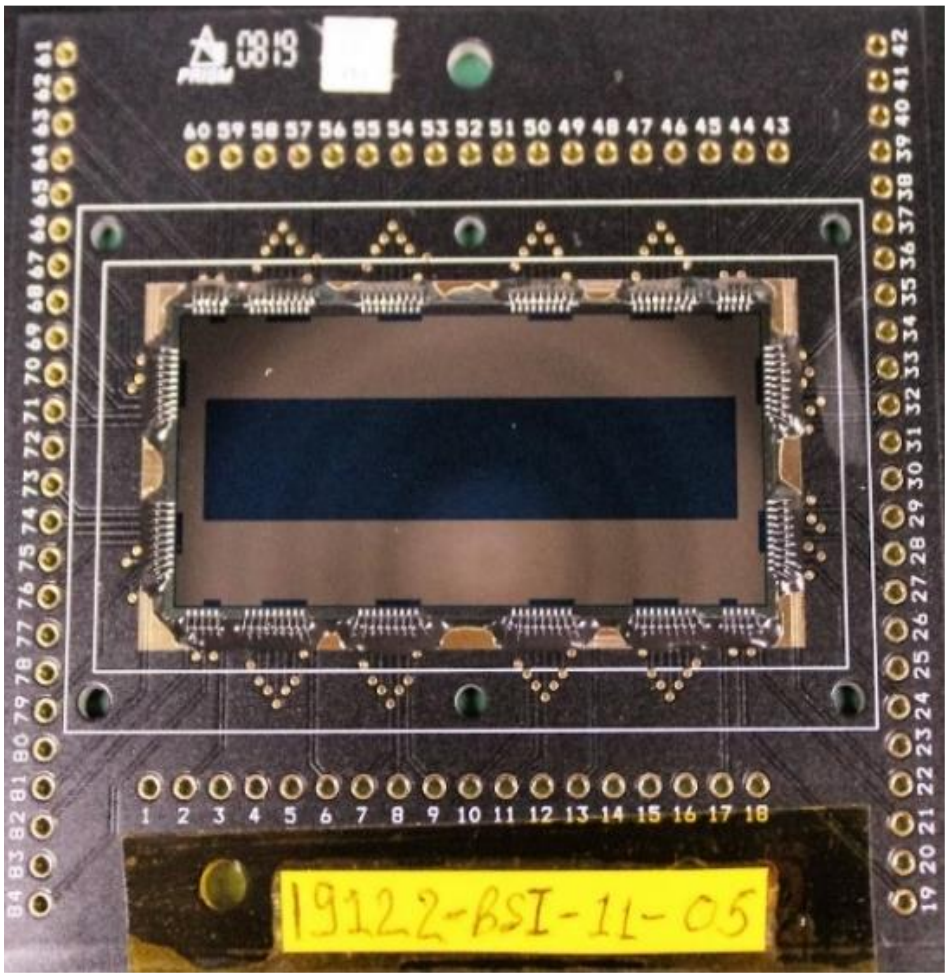

Figure 8. Image of a Back Side Illuminated (BSI) COB packaged detector.

The characterization test set-up is assembled consisting of uniform light source, light source power meter, DC voltage sources, drive electronic board, acquisition board and acquisition software. The light source is equipped with integrating sphere to have uniform output flux throughout aperture with added capability to adjust the intensity of output flux (Figure 10).

Once the full electronic chain is verified with detector, Light Transfer Characteristic (LTC) is assessed by varying the input light flux and measuring the corresponding detector output. Photon Transfer Curve (PTC) is obtained by plotting detector noise in output signal with corresponding output signal. The various detector performance parameters such as output linearity, charge to voltage conversion gain, pixel full well capacity are evaluated from LTC and PTC measurement.

The initial LTC and PTC test results for developed BSI detector is shown in Figure 11. The LTC curve for BSI CCD detector shows that output signal is linear with input light flux (R^2=0.999) until the detector reaches saturation. For a photon noise limited system, the variance in PTC curve increases with output signal up to detector saturation. The output signal where variance begins to decrease, represents detector saturation output. The slope of linear region gives the conversion gain, which is 1.3 µV/e for this detector.

From Figure 11, it becomes evident that the PTC curve drops after reaching approximately 820 mV. The corresponding Full Well Capacity (FWC) is ~630 Ke^-. As the designed FWC value is >1000 ke^-, so the BSI CCD falls significantly short of the designed value. So, in next session, the detailed investigation of reason behind lower FWC is presented.

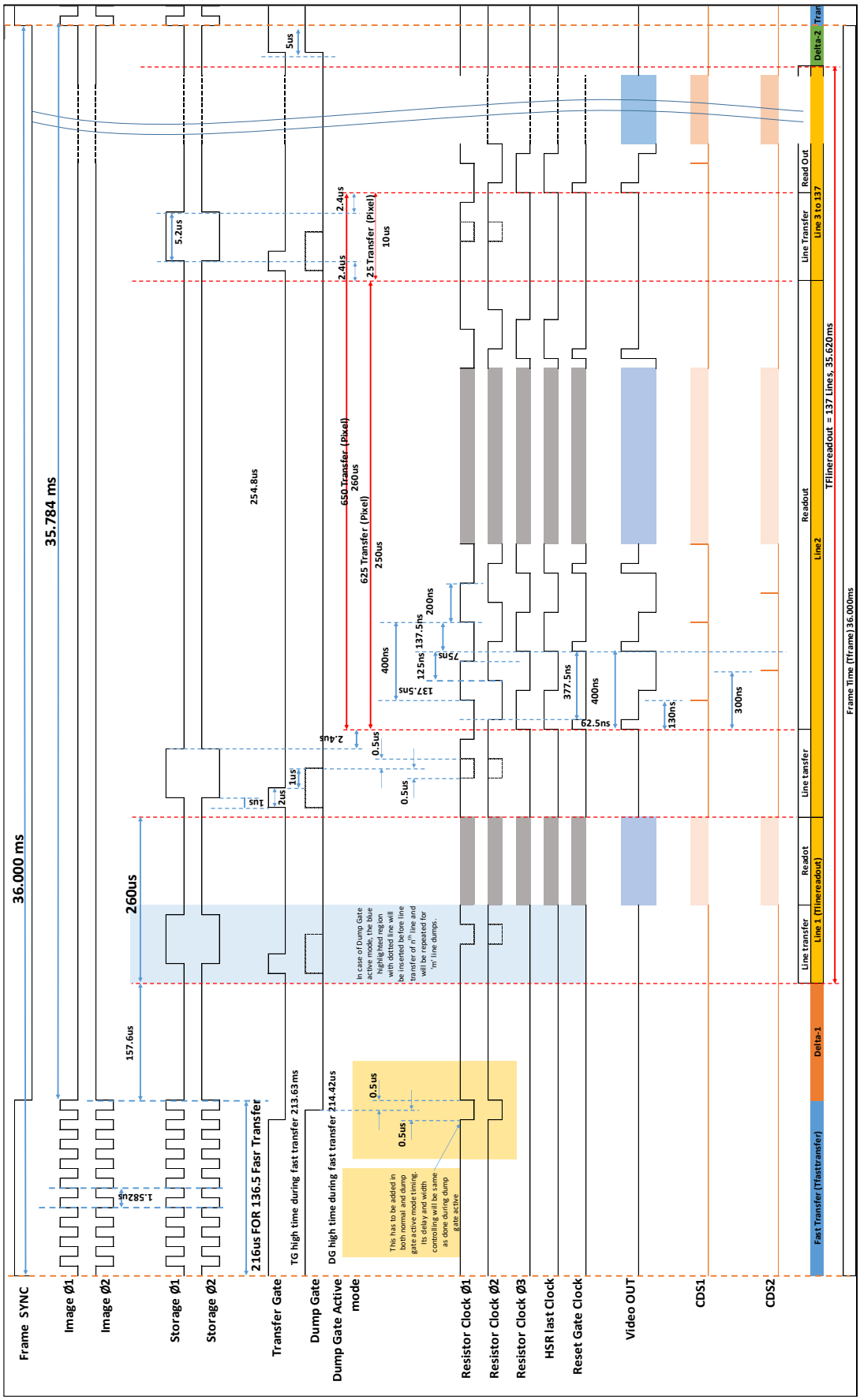

Figure 9. Clocks timing pattern for default operation. The dump gate is ‘ ON’ only at fast transfer duration. The dump gate active mode is also included with dotted lines but not applicable in default mode of operation.

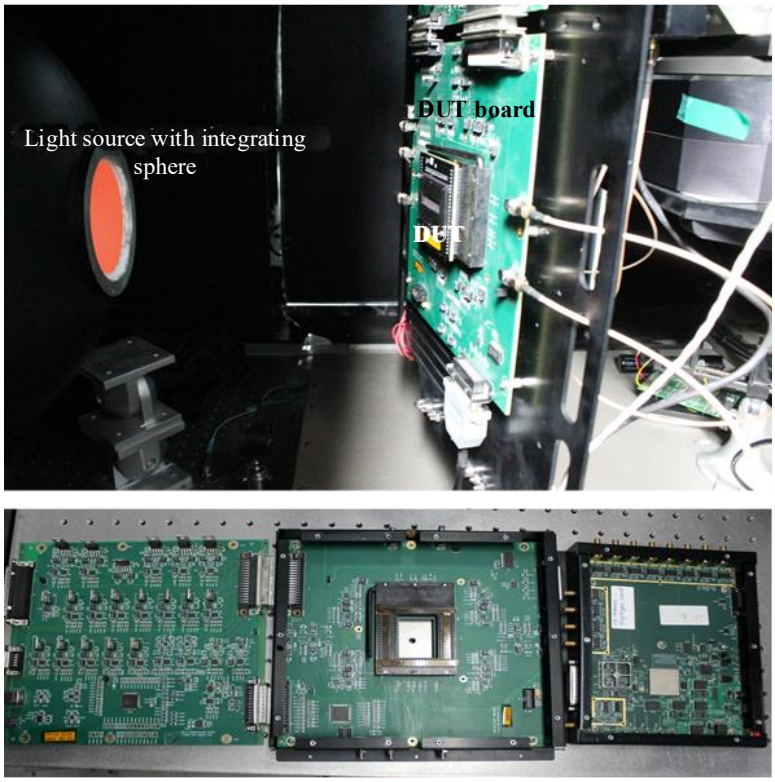

Figure 10. Detector characterization set-up and detector drive electronics boards.

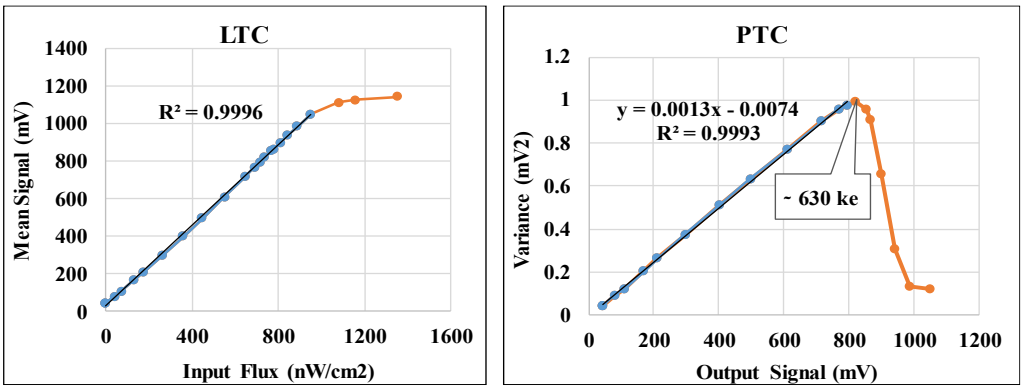

Figure 11. LTC and PTC plots for BSI CCD detector.

Investigation of Root Cause of Lower FWC in BSI CCD

The FWC measured by LTC and PTC plots gives FWC of lowest section among Floating Diode (FD) node, Horizontal Shift Register (HSR), Storage region and imaging region. In design phase, generally progressive section in charge transfer direction is designed having higher FWC than that of preceding one. We further estimate FWC of FD node, HSR, storage region and image region individually. To estimate the FWC of each section, signal charge binning in each individual section is employed.

Floating Diffusion (FD) Full Well Capacity Estimation

To estimate full well capacity of floating node, signal binning at FD node at fixed illumination level is used. The following timing diagram in Figure 12 illustrates the signal binning for four pixels at FD node. The timing of all clocks are same as shown in Figure 8 except reset clock. Here the reset clock is skipped for consecutive pixels, allowing accumulation of signal charges at FD node until saturation occurs. As the signal charges are accumulated at FD node without pixel reset, the video reference

voltage decreases with successive pixel binning as shown in the left image in Figure 12 for four pixels binning. The plot of binned output signal in mV vs. number of pixel's charge binning is shown in right side plot of Figure 12. It can be clearly seen that binned signal output deviates from linearity after reaching 2500 mV which indicates FD saturation. Consequently, the floating diffusion has ample FWC, surpassing 2500 mV.

Horizontal Shift Register (HSR) Full Well Capacity Estimation

In order to estimate full well capacity of HSR, signal from multiple successive storage rows are binned in HSR and then sequentially readout. Specific timing for binning signal charges from two rows is shown in Figure 13. In this timing diagram, HSR clocks are kept temporally on hold to receive the signal from two storage rows. On first transfer gate pulse, signal from adjacent storage row is transferred to HSR, keeping HSR phases at same potential, again next TG pulse transfers signal from the next adjacent storage row to HSR. Initially, the illumination level is kept low such that signal level remains a fraction of HSR FWC.

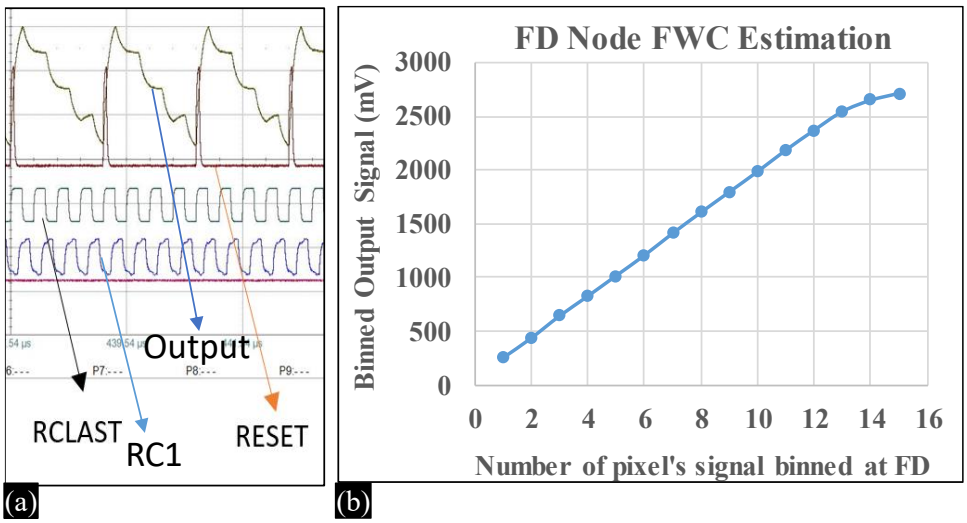

Figure 12. (a) Timing diagram for register clocks (RC, RCLAST) and reset clock and corresponding output waveform for estimating the FWC of FD node.
(b) Plot of output signal vs number of pixels signal binning at FD node.

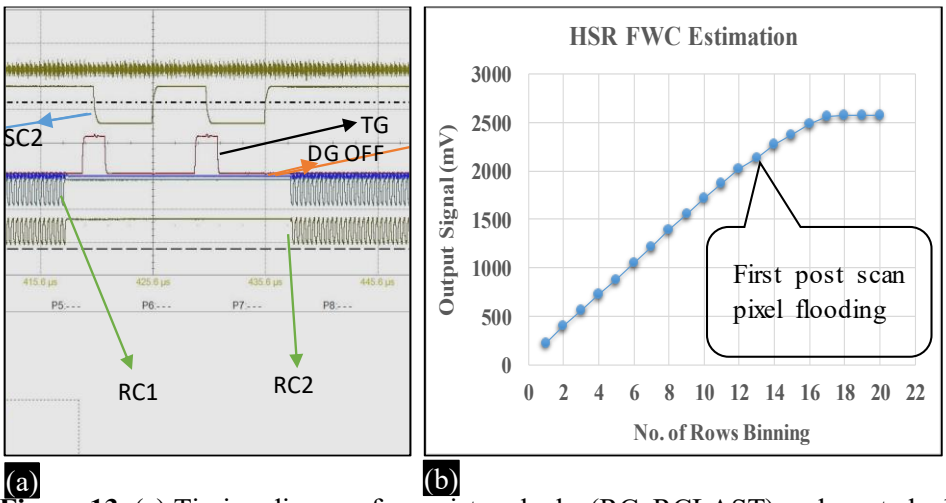

Figure 13. (a) Timing diagram for register clocks (RC, RCLAST) and reset clock and corresponding output waveform for estimating the FWC of FD node.
(b) Plot of output signal vs. number of pixels signal binning at FD node.

The plot shown on right image in Figure 13 represents binned output signal vs. number of rows binned. From the plot it is clear that binned output flattens after reaching 2500 mV. However, charge signal spilled over the first HSR post-scan pixel at 13 rows of binning. As charge signal spillage to first post scan pixel indicates the saturation of HSR pixels, therefore HSR pixels have FWC approximately 2100 mV. The designed FWC for the Floating Diode (FD) is set higher than that of the HSR to ensure the accurate sensing of charge signals up to the FWC of the HSR. As per measurement, both FD and HSR have adequate FWC, next we will evaluate the FWC of storage pixels.

Storage and Image Pixels Full Well Capacity Estimation

To estimate full well capacity of storage pixels, signal from multiple consecutive storage rows are binned in first storage row (which is adjacent to TG). This is achieved by keeping TG turned off and clocking increasing number of storage cycles. Specific timing for two lines binning is shown in Figure 14. The timing shown is region of slow transfer from storage region to HSR, as first time storage clock (SC2) goes low, TG is held at low potential, so signal charge is still in last row of storage (adjacent to TG). As the storage pixel has two-phase structure, it can store signal charge even at low potential. When SC2 goes high again at second time, the signal charges from two adjacent rows get binned and transferred to HSR once the TG goes high.

Similarly, for successive rows binning, consecutive TG pulse is skipped. The binned output vs. number of storage row binned is shown in right image of Figure 14. It becomes evident that binned output flattens only after reaching 900 mV, indicating that storage pixels have full well capacity approximately 900 mV. This finding signifies that the storage pixel has a lower full well capacity, akin to the Full Well Capacity (FWC) measured from the Photon Transfer Curve (PTC). As the image and storage pixels have similar structure, the image pixels are expected to exhibit similar FWC.

However, we have estimated FWC of image pixels separately by signal binning of multiple successive image rows in the first image row (adjacent to storage region) by clocking successive more number of image clocks and holding storage clocks for same number of cycles at the start of the fast transfer from image region to storage region. The measured FWC of image pixel is similar to storage pixel.

In back side processing, the substrate of the device is removed by chemical-mechanical polishing and then shield metal deposited. The substrate plays a vital role for providing reference potential. The removal of substrate can lead to substrate bounce effects which will be discussed in next section.

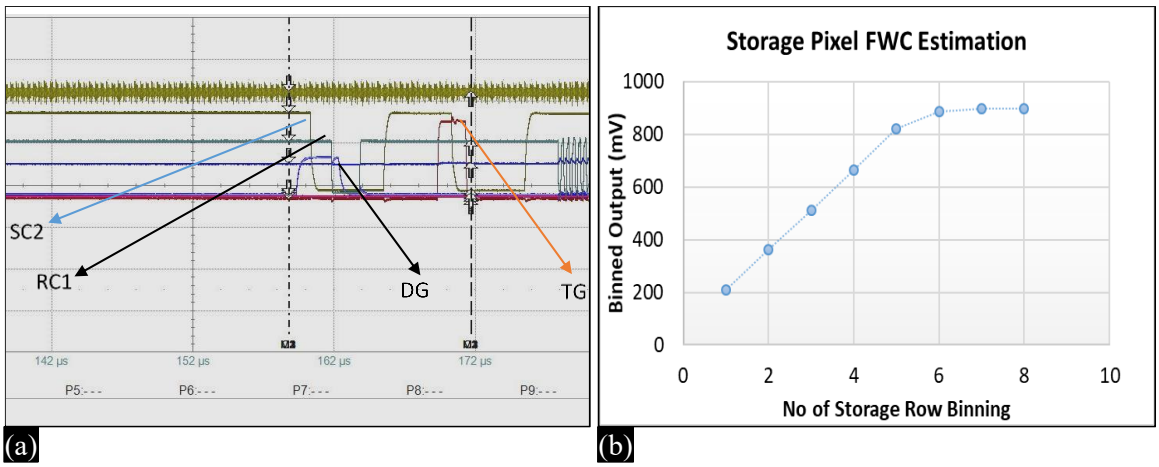

Figure 14. (a) Timing diagram for Storage clock 2 (SC2), Transfer Gate (TG), Dump Gate (DG), and Register Clocks (RC1) for estimating the FWC of storage pixels. (b) The Binned output signal vs number of rows binning is shown in right image.

Optimization of Full Well Capacity of BSI CCD

As inferred from results of previous section, the storage and image pixel have significantly lower FWC than designed values. The image and storage clocks have high capacitive loads (designed extracted values, 8.4 nF for image section clocks and 8.9 nF for storage section clocks) and image to storage transfer is fast (700 kHz) to reduce the smear. Clocking the gate is analogous to charging and discharging a capacitor. Displacement current associated to clocking must flow in and out of the device through the substrate [15]. For the n-channel front illuminated CCD, this current in the form of holes can freely flow in and out of CCD through low resistance substrate region. While in back illuminated CCD, due to absence of substrate, hole must travel laterally through epitaxial material or channel stop to reach ground. As a result, a ground impedance exists, causing an IR drop although the design has included the substrate connection to reduce the impedance. The high frequency clock with high capacitive load can elevate the voltage reference to few volts, which is termed as "substrate bounce". Substrate bounce is an important mechanism that can affect high-speed operation and degrades the full well capacity [16]. As depicted in Figure 15, the clock signal from clock driver propagates to CCD through wave shaping network (Rws and Cws) which adjusts rise/fall of clocks [17].

Inside the detector, the clock signal encounters resistance (Rpix) of metal tracks and capacitance (Cpix) from the oxide and depletion region. The substrate bounce perturbs the substrate reference and dramatically degrades full well capacity. The substrate bounce problem is prevalent in image and storage clocks because of high capacitance and related currents. The amplitude of substrate bounce is extremely dependent on image and storage clock amplitude. The clock with higher amplitude encounters higher substrate bounce phenomena [16]. Taking the substrate bounce phenomena into consideration, we have reduced the image and storage clocks amplitude to 10 V from default 12 V by lifting clock low level to 2 V. The Figure 16(a) shows LTC and Figure 16(b) shows PTC plot after clock amplitude optimization along with initial PTC plot. Elevating the low level of image and storage clocks, effectively reduces the substrate bounce hence the LTC and PTC curves result in higher saturation voltage (~1300 mV).

Consequently, the corresponding FWC is around 1100 ke, a value closely aligned with designed value. The Figure 16(c) also demonstrates that altering both the low and high levels of the image and storage clocks while maintaining a constant amplitude of 10 V results in a nearly consistent FWC. The first plot in Figure 16(c) shows PTC at image and storage clock low level 2 V and high level 12 V, then in subsequent plots both the low and high levels are reduced by 0.5 V while retaining the 10 V amplitude. The BSI device meets FWC designed values of 1 Me^- even when low level in 0 V (grounded) and high level of 10 V (hence effectively 10 V amplitude). The Figure 16(d) shows measured Quantum Efficiency (QE) from 400 to 1000 nm wavelength range, in steps of 10 nm. The measured quantum efficiency is 32% at 400 and 1000 nm both along with higher than 30% at intermediate wavelengths, which fulfills the QE requirement.

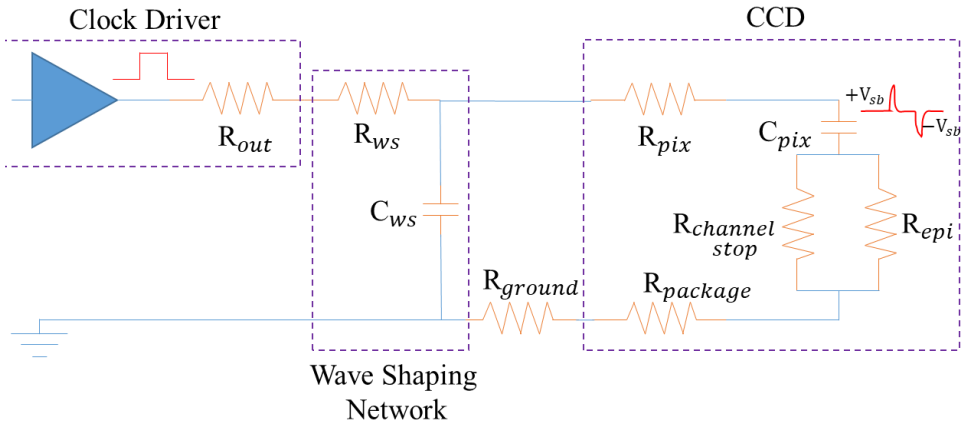

Figure 15. Representative schematic of CCD clock signal drive circuit and impedances responsible for substrate bounce.

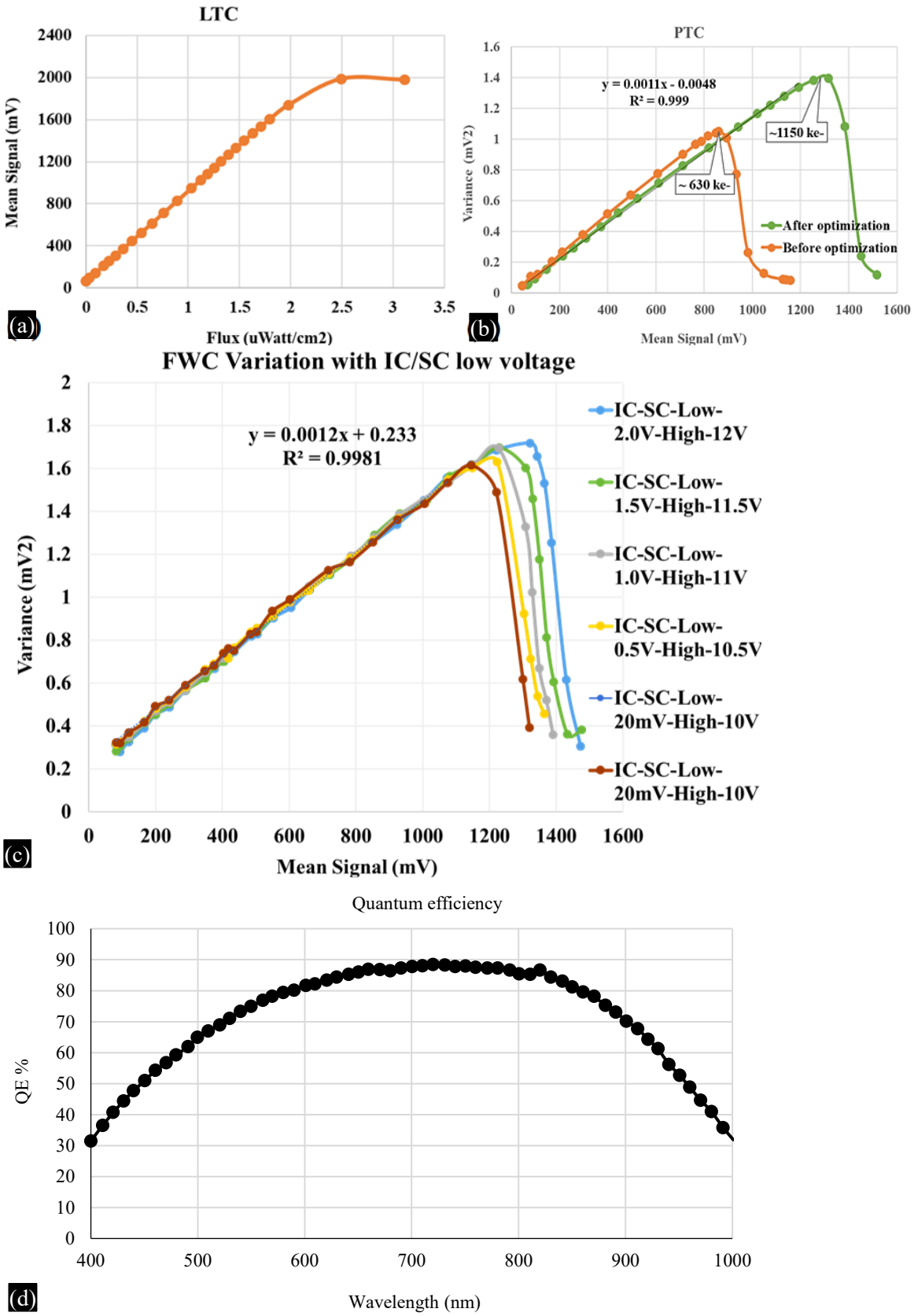

Figure 16. (a) LTC and (b) PTC curve of BSI CCD detector after reducing vertical clocks amplitude. (c) PTC at different low and high level of vertical clocks but have same amplitude (d) Quantum Efficiency plot from 400 to 1000 nm of a BSI detector after clock.

CONCLUSION

We have represented the detailed chip design of a frame transfer CCD including image, storage, HSR and peripheral circuits along with various design optimization to achieve targeted device performance. Additionally, we have outlined the initial characterization process of a CCD and expounded upon the subsequent performance optimization procedures. The measured performance is in good agreement with designed values except the Full Well Capacity (FWC). The detailed investigation is done to find out root cause behind the lower FWC of BSI CCD. The lower FWC of BSI was attributed to the substrate bounce issue. Consequently, the target FWC>1 Me^- is achieved by optimizing the amplitude of vertical clocks. The measured QE is 32% at 400 and 1000 nm both, against the requirement of 30% at 400 nm and 20% at 1000 nm. To maintain conciseness in the study, we have solely presented the FWC optimization, while it is worth noting that other performance parameters were also optimized.

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